CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

1. A method of forming a metal-insulator-silicon (MIS) capacitor comprising the steps of:

(a) implanting a bottom electrode into a surface of a Si-containing substrate;

(b) forming a high-k dielectric over at least a portion of said bottom electrode, said high-k dielectric having a dielectric constant of greater than about 8.0; and

(c) forming a doped Si-containing electrode over said high-k dielectric, wherein said doped Si-containing electrode comprises an intrinsic base polysilicon layer of a bipolar device.

2. The method of Claim 1 wherein step (a) includes a high-dose reach-thru implant which provides a doped region having a dopant concentration of about 1E19 atoms/cm^3 or above

3. The method of Claim 1 wherein following said implant step said bottom electrode is annealed in an inert gas.

4. The method of Claim 1 wherein said high-k dielectric is formed by a deposition process selected from the group consisting of low pressure chemical vapor deposition, atomic layer chemical vapor deposition, rapid thermal chemical vapor deposition, plasma-assisted chemical vapor deposition, physical vapor deposition, sputtering, plating, evaporation and chemical solution deposition.

5. The method of Claim 1 wherein said high-k dielectric is a binary metal oxide, a silicate, aluminate, or oxynitride of a binary metal oxide, or a perovskite oxide.

6. The method of Claim 5 wherein said high-k dielectric is a binary metal oxide or an aluminate of a binary metal oxide.

7. The method of Claim 6 wherein said high-k dielectric is Al_2O_3.

8. The method of Claim 1 wherein said high-k dielectric has a thickness of from about 50 to about 1000 Å.

9. The method of Claim 1 wherein a diffusion barrier layer is formed on said bottom electrode prior to formation of said high-k dielectric, on said high-k dielectric or both.

10. The method of Claim 1 wherein said high-k dielectric and said doped Si-containing electrode are patterned after performing step (c).

11. The method of Claim 10 wherein said patterning includes lithography and etching.

12. The method of Claim 1 wherein said doped Si-containing electrode comprises poly SiGe.

13. The method of Claim 1 wherein said doped Si-containing electrode is formed by deposition and ion implantation or by an in-situ doping deposition process.

14. The method of Claim 10 wherein spacers are formed on exposed sidewalls of said patterned high-k dielectric and said patterned doped Si-containing electrode.

15. The method of Claim 11 wherein an amorphization step follows said lithography step.

16. A MIS capacitor integrated with a bipolar device comprising an implanted bottom electrode formed in a surface of a Si-containing substrate; a high-k dielectric having a

dielectric constant of greater than about 8 formed on a portion of said implanted bottom electrode; and a doped Si-containing electrode formed on said high-k dielectric, wherein said doped Si-containing electrode comprises an intrinsic base polysilicon layer of a bipolar device.

17. The MIS capacitor of Claim 16 wherein said high-k dielectric is a binary metal oxide, a silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite oxide.

18. The MIS capacitor of Claim 17 wherein said high-k dielectric is a binary metal oxide or an aluminate of a binary metal oxide.

19. The MIS capacitor of Claim 18 wherein said high-k dielectric is Al_2O_3.

20. The MIS capacitor of Claim 16 wherein said doped Si-containing electrode is composed of poly SiGe.

21. The MIS capacitor of Claim 16 wherein spacers are present on any exposed sidewalls of said high-k dielectric and said doped Si-containing electrode.

22. The MIS capacitor of Claim 16 wherein a diffusion barrier layer is present between said bottom electrode and said high-k dielectric, between said high-k dielectric and said doped Si-containing electrode, or between said bottom electrode and said high-k dielectric and between said high-k dielectric and said doped Si-containing electrode.

23. A method of fabricating a poly-poly capacitor comprising the steps of:

(a) forming a base polysilicon layer over at least isolation regions;

(b) forming a high-k dielectric over at least a portion of isolation regions, wherein said high-k dielectric has a dielectric constant of greater than about 8.0; and

(c) forming a doped Si-containing electrode over said high-k dielectric, wherein said doped Si-containing electrode comprises an intrinsic base polysilicon layer of a bipolar device.

24. The method of Claim 23 wherein said isolation regions are local oxidation of silicon regions or trench isolation regions.

25. The method of Claim 23 wherein said base polysilicon layer is formed by a deposition process selected from the group consisting of chemical vapor deposition, plasma-assisted chemical vapor deposition, sputtering evaporation, and chemical solution deposition.

26. The method of Claim 23 wherein said base polysilicon layer is doped by ion implantation.

27. The method of Claim 23 wherein said base polysilicon layer is comprised of poly SiGe.

28. The method of Claim 23 wherein said high-k dielectric is formed by a deposition process selected from the group consisting of low pressure chemical vapor deposition, atomic layer chemical vapor deposition, rapid thermal chemical vapor deposition, plasma-assisted chemical vapor deposition, physical vapor deposition, sputtering, plating, evaporation and chemical solution deposition.

29. The method of Claim 23 wherein said high-k dielectric is a binary metal oxide, a silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite oxide.

30. The method of Claim 29 wherein said high-k dielectric is a binary metal oxide or an aluminate of a binary metal oxide.

31. The method of Claim 30 wherein said high-k dielectric is Al_2O_3.

32. The method of Claim 23 wherein said high-k dielectric has a thickness of from about 50 to about 1000 Å.

33. The method of Claim 23 wherein a diffusion barrier layer is formed on said bottom electrode prior to formation of said high-k dielectric, on said high-k dielectric or both.

34. The method of Claim 23 wherein said high-k dielectric and said doped Si-containing electrode are patterned after performing step (c).

35. The method of Claim 34 wherein said patterning includes lithography and etching.

36. The method of Claim 23 wherein said doped Si-containing electrode comprises poly SiGe.

37. The method of Claim 23 wherein said doped Si-containing electrode is formed by deposition and ion implantation or by an in-situ doping deposition process.

38. The method of Claim 34 wherein spacers are formed on exposed sidewalls of said patterned high-k dielectric and said patterned doped Si-containing electrode.

39. The method of Claim 35 wherein an amorphization step follows said lithography step.

40. A poly-poly capacitor comprising a bottom polysilicon electrode formed over isolation regions that are present in a Si-containing substrate; a high-k dielectric

having a dielectric constant of greater than about 8 formed on a portion of said bottom electrode; and a doped Si-containing electrode formed on said high-k dielectric, wherein said doped Si-containing electrode comprises an intrinsic base polysilicon layer of a bipolar device.

41. The poly-poly capacitor of Claim 40 wherein said bottom polysilicon electrode is composed of poly SiGe.

42. The poly-poly capacitor of Claim 40 wherein said high-k dielectric is a binary metal oxide, a silicate, aluminate or oxynitride of a binary metal oxide, or a perovskite oxide.

43. The poly-poly capacitor of Claim 42 wherein said high-k dielectric is a binary metal oxide or an aluminate of a binary metal oxide.

44. The poly-poly capacitor of Claim 43 wherein said high-k dielectric is Al_2O_3.

45. The poly-poly capacitor of Claim 40 wherein said doped Si-containing electrode is comprised of poly SiGe.

46. The poly-poly capacitor of Claim 40 wherein spacers are present on any exposed sidewalls of said high-k dielectric and said doped Si-containing electrode.

47. The poly-poly capacitor of Claim 40 wherein a diffusion barrier layer is present between said bottom electrode and said high-k dielectric, between said high-k dielectric and said doped Si-containing electrode, or between said bottom electrode and said high-k dielectric and between said high-k dielectric and said doped Si-containing electrode.